**TSPi Plan Summary: Form SUMP**

Name **基于android家谱树的设计与实现** Date  **2016/05/18**

Team  **Team 8**  Instructor  **张笑燕**

Part/Level  Cycle  **1**

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| **Product Size** | **Plan** | **Actual** |
| Requirements pages (SRS) | 25 | 28 |
| Other text pages | 60 | 45 |
| High-level design pages (SDS) | 20 | 23 |
| Base LOC (B) (measured) | 100 | 200 |
| Modified LOC (M) | 250 | 120 |
| Added LOC (A) | 1000 | 2000 |
| Reused LOC (R) | 200 | 300 |
| Total New and Changed LOC (N) | 1250 | 2120 |
| Total LOC (T) | 1300 | 3200 |
| Total new Reuse LOC | 300 | 420 |
| Estimated Object LOC (E) | 4000 | - |
| Upper Prediction Interval (70%) |  | - |
| Lower Prediction Interval (70%) |  | - |

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| **Time in Phase (hours)** | **Plan** | **Actual** | **Actual %** |
| Management and miscellaneous | 5 | 8 | 3.43 |
| Launch | 5 | 6 | 2.58 |
| Strategy and planning | 10 | 12 | 5.15 |
| Requirements | 15 | 19 | 8.15 |
| System test plan | 2 | 5 | 2.15 |
| Requirements inspection | 2 | 4 | 1.71 |
| High-level design | 20 | 18 | 7.73 |
| Integration test plan | 3 | 3 | 1.29 |
| High-level design inspection | 4 | 7 | 3.00 |
| Implementation Planning | 2 | 3 | 1.29 |
| Detailed design | 20 | 26 | 11.16 |
| Detailed design review | 4 | 5 | 2.15 |
| Test development | 5 | 10 | 4.29 |
| Detailed design inspection | 4 | 5 | 2.15 |
| Code | 50 | 60 | 25.75 |
| Code review | 5 | 2 | 0.86 |
| Compile | 5 | 10 | 4.29 |
| Code inspection | 10 | 4 | 1.71 |
| Unit test | 3 | 3 | 1.29 |
| Build and integration | 3 | 3 | 1.29 |
| System test | 5 | 5 | 2.15 |
| Documentation | 4 | 5 | 2.15 |
| Postmortem | 10 | 10 | 4.29 |
| Total | 196 | 233 | 100.00 |
| Total Time UPI (70%) |  |  |  |
| Total Time LPI (70%) |  |  |  |

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| **Defects Injected** | **Plan** | **Actual** | **Actual %** |
| Strategy and planning | 5 | 5 | 10.00 |
| Requirements | 4 | 4 | 8.00 |
| System test plan | 2 | 1 | 2.00 |
| Requirements inspection | 0 | 0 | 0.00 |
| High-level design | 5 | 9 | 18.00 |
| Integration test plan | 7 | 8 | 16.00 |
| High-level design inspection | 0 | 0 | 0.00 |
| Detailed design | 3 | 3 | 6.00 |
| Detailed design review | 0 | 0 | 0.00 |
| Test development | 5 | 5 | 10.00 |
| Detailed design inspection | 0 | 0 | 0.00 |
| Code | 10 | 14 | 28.00 |
| Code review | 0 | 0 | 0.00 |
| Compile | 0 | 0 | 0.00 |
| Code inspection | 0 | 0 | 0.00 |
| Unit test | 0 | 0 | 0.00 |
| Build and integration | 2 | 1 | 2.00 |
| System test | 0 | 0 | 0.00 |
| Total Development | 43 | 50 | 100.00 |

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| **Defects Removed** | **Plan** | **Actual** | **Actual %** |
| Strategy and planning | 0 | 0 | 0.00 |
| Requirements | 0 | 0 | 0.00 |
| System test plan | 0 | 0 | 0.00 |
| Requirements inspection | 10 | 10 | 20.00 |
| High-level design | 0 | 0 | 0.00 |
| Integration test plan | 0 | 0 | 0.00 |
| High-level design inspection | 11 | 12 | 24.00 |
| Detailed design | 0 | 0 | 0.00 |
| Detailed design review | 4 | 6 | 12.00 |
| Test development | 0 | 0 | 0.00 |
| Detailed design inspection | 4 | 5 | 10.00 |
| Code | 0 | 0 | 0.00 |
| Code review | 6 | 7 | 14.00 |
| Compile | 4 | 5 | 10.00 |
| Code inspection | 1 | 2 | 4.00 |
| Unit test | 1 | 1 | 2.00 |
| Build and integration | 0 | 0 | 0.00 |
| System test | 2 | 2 | 4.00 |
| Total Development | 43 | 50 | 100.00 |